

# Analog IC Design Homework 2 (1/5)

## ● 題目: Two-stage CMOS OPAMP and bias circuit

1. 可使用0.18 $\mu\text{m}$ , 16nm 或其他更先進製程 SPICE Model (須先至Moodle登記)
2. 請參考P.2 Fig. 1所示之偏壓電路。你認為圖中之電路有何問題？是否需要修改或加入其他輔助電路？請說明理由。並手算設計Fig. 1所示之偏壓電路與輔助電路(如果需要)，使全部的branch電流總和不超過15 $\mu\text{A}$ ，且  $V_{\text{eff1}\sim 2} > 0.15\text{V}$  與  $V_{\text{eff6}} > 0.15\text{V}$ 。
3. 請使用 2. 設計之偏壓電路並手算設計如P.2 Fig. 2所示的two-stage CMOS OPAMP，相關規格如下：
  - ◆ Unity-gain frequency  $\geq 230\text{ MHz}$
  - ◆ Phase margin( $\phi_M$ ):  $60^\circ \leq \phi_M \leq 66^\circ$
  - ◆ DC gain  $\geq 64\text{ dB}$
  - ◆ Slew rate (rise and fall)  $\geq 110\text{ V}/\mu\text{s}$
  - ◆ Load capacitance = 2 pF
  - ◆ Power supply  $V_{\text{DD}} = 1.8\text{V}$   
(16nm ADFP  $V_{\text{DD}} \leq 1.05\text{V}$ )
4. 使用HSPICE(以testbench\_AC.sp, testbench\_SR.sp測試)驗證所設計之Bias circuit 和 two-stage CMOS OPAMP，比較並分析手算及HSPICE驗證的結果。

## ● Deadline (過補交期限或抄襲者以0分計算。)

- ◆ 10/12/2025(Sun.)11:59:59 pm，補交期限10/15/2025 8:30:00 am前遲交1天扣20分 (以滿分100分計)

## ● 注意事項

- ◆ 使用0.18 $\mu\text{m}$ 製程模擬須符合助教所規定之規格
- ◆ 使用16nm或更先進製程模擬可自定規格，規格愈佳可獲愈高分
- ◆ 一人一組，檔案請壓縮成zip檔並取名為 HW#\_學號，例：HW2\_N26000000.zip。
- ◆ 將檔案(含Word報告、Powerpoint繪圖及HSpice程式碼(.sp檔與.cir檔))上傳至moodle。
- ◆ 字體大小12pt (中文: 標楷體，英文: Times New Roman)。
- ◆ 根據IEEE上傳規定，請將圖片解析度設置為300dpi。建議上傳文件大小為1MB。

# Analog IC Design Homework 2 (2/5)

- Circuit diagram

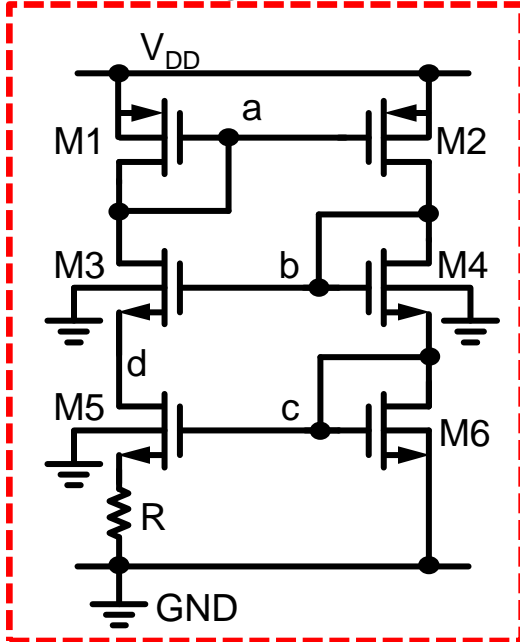


Fig. 1 : Bias Circuit

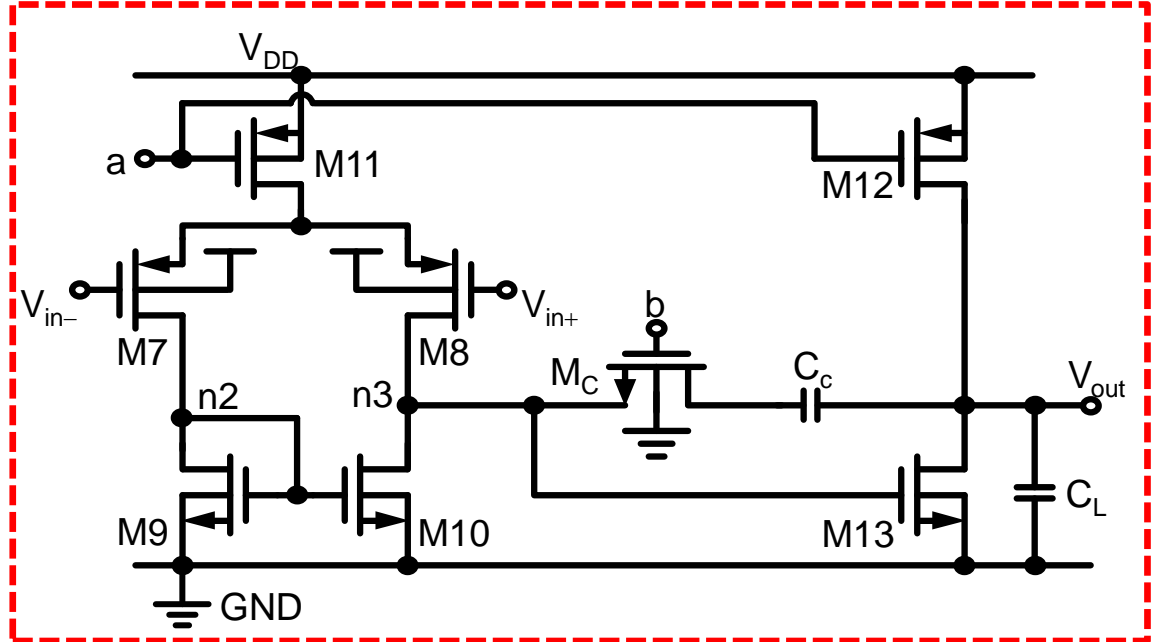


Fig. 2 : Two Stage OPAMP

- Note:

- ◆ Follow design rules of maximum and minimum transistor width and length.
  - $L_{\min}=0.18\mu\text{m}$ ,  $L_{\max}=50\mu\text{m}$ ,  $W_{\min}=0.25\mu\text{m}$ ,  $W_{\max}=100\mu\text{m}$
- ◆ External voltage or current sources are not allowed except 1.8V supply voltage and input common mode voltage.
- ◆ Input common mode voltage 請自行設計於合理範圍內
- ◆ 請使用 Cadence Virtuoso 建立 Schematic，並轉出 .cir 檔進行驗證

# Analog IC Design Homework 2 (3/5)

- Your report should include

- ◆ 推導及設計過程

- ◆ HSPICE執行驗證結果

- HSPICE執行驗證結果含各電晶體之節點電壓與偏壓電流(須如P.5範例標示於電路圖上)，且須附上電晶體操作區，以利判別電晶體是否操作在適當的操作區
- Note: 以往有人以.measure將phase margin或者unity gain freq.直接show在SPICE輸出文字檔中，由於文字容易被編輯與修改，因此本作業需附上波德圖(含Gain大小與相位)和波形圖(Slew rate)，並於圖中標示驗證結果

- ◆ Virtuoso schematic

- 須附上.cir檔與電路圖

- ◆ Calculating the input common mode range and output swing

- ◆ Area (should include bias circuit & two stage opamp)

- MOSFET: Please calculate the sum of the  $W \cdot L$  for all the MOS used in the designed circuit.

$$A_{MOS} = \sum W_i \times L_i$$

- Capacitor: Just show the capacitance (if used)
- Resistor: Just show the resistance (if used)

- ◆ Total current and power consumption (should include bias circuit & two stage opamp)

- ◆ 規格表(如P.4下方所示)

# Analog IC Design Homework 2 (4/5)

- 評分標準

- ◆ 自行撰寫.sp檔將不予計分。完全沒有設計過程之討論，只有模擬結果者視情況扣分。
- ◆ 節點與電晶體名稱請使用如P.2所示之名稱。
- ◆ 報告清楚描述設計流程，並附上計算過程、各節點電壓與branch電流大小、Veff結果
  - 需附圖(附圖請反白)，請參考P.5的範例。
- ◆ 報告以內容完整與頁數精簡為原則，有額外探討分析者分數較高。
- ◆ 在達到作業規格前提下，較小power consumption 和較小 area，分數較高。

- 請於HW2報告最後一頁加入下表，以便助教批改作業

姓名_學號		
DC gain (dB)		
Unit-gain bandwidth (MHz)		
Phase margin		
Slew rate	Rising (V/ $\mu$ s)	
	Falling (V/ $\mu$ s)	
Input common-mode range		
Output swing		
Area ( $\mu\text{m}^2$ )		
Total current ( $\mu\text{A}$ )		

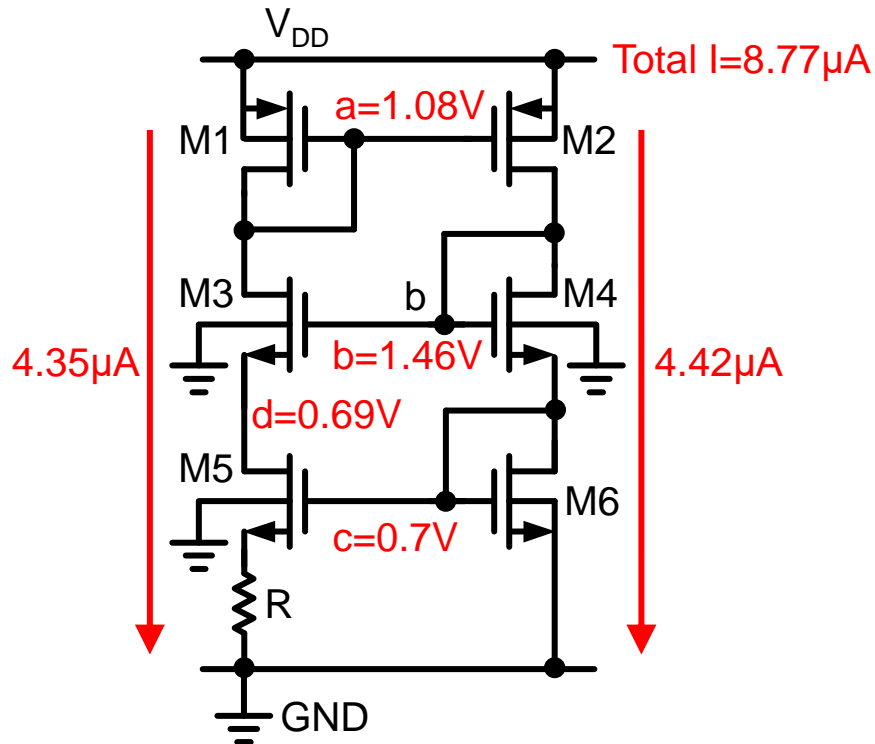
# Analog IC Design Homework 2 (5/5)

● 電晶體標號請與作業說明所給附圖(P.2 Fig. 1 & Fig. 2)一致

● 作業附圖範例 (數值並非此次作業的結果)

◆ 各節點電壓與branch電流大小

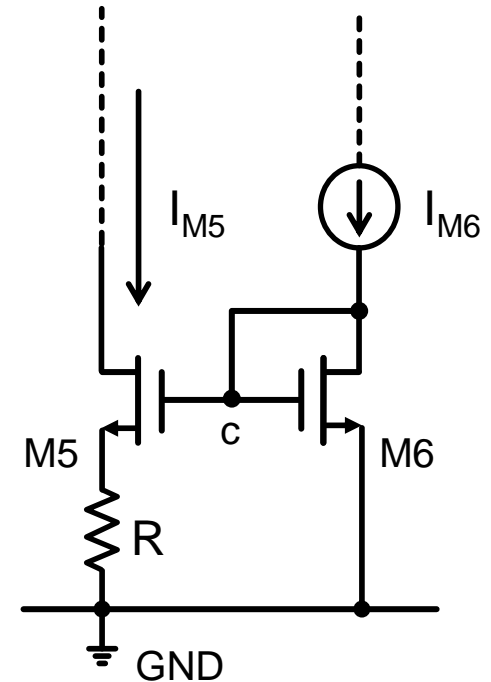
◆  $V_{\text{eff}}$  結果 (可由 .lis 檔裡獲得)



element	0:m1	0:m2	0:m3	0:m4	0:m5	0:m6
model	0:p_18.1	0:p_18.1	0:p_18.1	0:p_18.1	0:n_18.1	0:n_18.1
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-4.3473u	-4.4180u	-4.3473u	-4.4180u	4.3261u	4.4180u
ibs	1.598e-21	1.624e-21	13.9675a	14.6963a	-25.1826a	-24.1428a
ibd	13.9643a	14.6930a	42.2872a	66.1813a	-97.2083a	-60.1641a
vgs	-725.0080m	-725.0080m	-768.2064m	-755.7124m	687.6708m	699.1690m
vds	-239.4341m	-251.9280m	-485.5739m	-882.7238m	796.5523m	398.4067m
vbs	0.	0.	239.4341m	251.9280m	-278.4397m	-266.9415m
vth	-507.7206m	-507.6434m	-569.5798m	-569.7012m	449.3836m	453.1541m
vdsat	-250.2910m	-250.3473m	-240.5100m	-230.5891m	240.1984m	245.8523m
vod	-217.2874m	-217.3646m	-198.6265m	-186.0112m	238.2872m	246.0149m
beta	171.8590u	171.8716u	165.3343u	165.7395u	141.9257u	141.8204u
gam eff	557.0845m	557.0845m	555.4377m	555.3567m	514.7198m	514.4379m
gm	27.8375u	28.6579u	32.4418u	34.7200u	31.1996u	30.4795u
gds	5.9959u	5.3391u	1.9385u	1.2406u	602.9213n	1.2151u
gmb	8.3425u	8.5761u	8.5525u	9.0131u	4.3764u	4.3676u
cdtot	602.2694a	595.6395a	516.0501a	481.1913a	419.0156a	455.6877a
cgtot	637.8033a	636.1121a	626.2839a	624.9136a	961.9485a	965.9698a
cstot	1.0546f	1.0547f	995.4309a	991.7572a	1.2412f	1.2437f
cbtot	1.1033f	1.1010f	974.6619a	938.1662a	891.8941a	923.0924a
cgs	472.5061a	472.3538a	473.5485a	471.8366a	787.5885a	790.1812a
cgd	128.0263a	125.9915a	116.8744a	116.3205a	89.1763a	92.5485a

# Appendix 1: Design Flow of Bias Circuit

- Step 1: 設定  $I_{M6}$  跟  $V_{\text{eff}6}$  → Find  $\left(\frac{W}{L}\right)_6$ 
  - ◆  $I_{M6} = \frac{1}{2} K n' \left(\frac{W}{L}\right)_6 (V_{\text{gs}6} - V_t)^\alpha (1 + \lambda V_{\text{DS}})$ 
    - $I_{M6} = \frac{1}{2} K n' \left(\frac{W}{L}\right)_6 V_{\text{eff}6}^\alpha (1 + \lambda V_{\text{DS}})$
- Step 2: 設定  $R$  → Find  $\left(\frac{W}{L}\right)_5$ 
  - ◆  $V_{\text{eff}6} = V_{\text{eff}5} + I_{M5} * R$
  - ◆  $I_{M5} = \frac{1}{2} K n' \left(\frac{W}{L}\right)_5 V_{\text{eff}5}^\alpha (1 + \lambda V_{\text{DS}})$
  - ◆  $I_{M5} = I_{M6}$
- Step 3: 設計  $M1 \sim M4$  之 size，使其操作在飽和區且  $V_{\text{eff}}$  符合限制
- Step 4: 設計 start up circuit



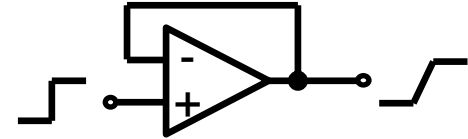
# Appendix 2: Design Flow of Two Stage OPAMP

- Step 1: 決定 $C_C$  (一般 $C_C$ 值會小於 $C_L$ ，太大會增大整體面積，太小會受到雜散電容的影響)
- Step 2: 由  $\varphi_m = 90^\circ - \tan^{-1}(f_t/f_{P2}) = 63^\circ \rightarrow f_{P2} = \frac{g_{m13}}{2\pi C_L} \approx 2 f_t$  且  $f_t = \frac{g_{m8}}{2\pi C_C} \rightarrow$  求得  $g_{m13}$
- Step 3: 由  $\text{Slew rate}(\text{SR}) < \frac{I_{11}}{C_C}$  &  $\frac{I_{12}}{C_C + C_L} \rightarrow C_C$  已知且SR須同時滿足兩公式  $\rightarrow$  求得  $I_{11}$ 、 $I_{12}$
- Step 4: 由DC Gain  $A_0 = \frac{\alpha I_{D8}}{V_{\text{eff8}}} (r_{o8} || r_{o10}) g_{m13} (r_{o12} || r_{o13}) \rightarrow I_{12} = I_{13} \rightarrow$  求得  $V_{\text{eff8}}$
- Step 5: 求出W/L (由上述條件可算出除了 $M_9 \sim M_{10}$ 跟 $M_C$ 的(W/L)值)
  - ◆  $M_9$ 跟 $M_{10}$ 的size決定 $V_{gs13}$ 的大小，調整(W/L) $_{9 \sim 10}$ 得到先前算出的 $V_{\text{eff13}}$
  - ◆  $M_C$ 的size可由設計好的 $R_C$ 值及公式  $R_C = \frac{1}{K_n' \left(\frac{W}{L}\right)_{M_C} (V_{GS_{M_C}} - V_t)}$  求出
- Note:  $n3$ 與 $V_{\text{out}}$ 的偏壓點會決定 $M_8$ 、 $M_{10}$ 、 $M_{12}$ 跟 $M_{13}$ 的操作區域
  - ◆ 如果 $V_{\text{out}}$ 的偏壓點過低，讓 $M_{13}$ 接近Linear region，會影響Gain的大小( $r_o$ 變小)
  - ◆ 若往下拉力量太強，只要稍微降低 $V_{gs13}$ ，就可以讓 $V_{\text{out}}$ 的偏壓點上升
  - ◆ 若  $V_{\text{OUT}}$  bias 偏低，可以  $M_9 \uparrow$ ,  $M_{10} \uparrow$  或  $M_{13} \downarrow$

# Appendix 3: Information of Slew Rate

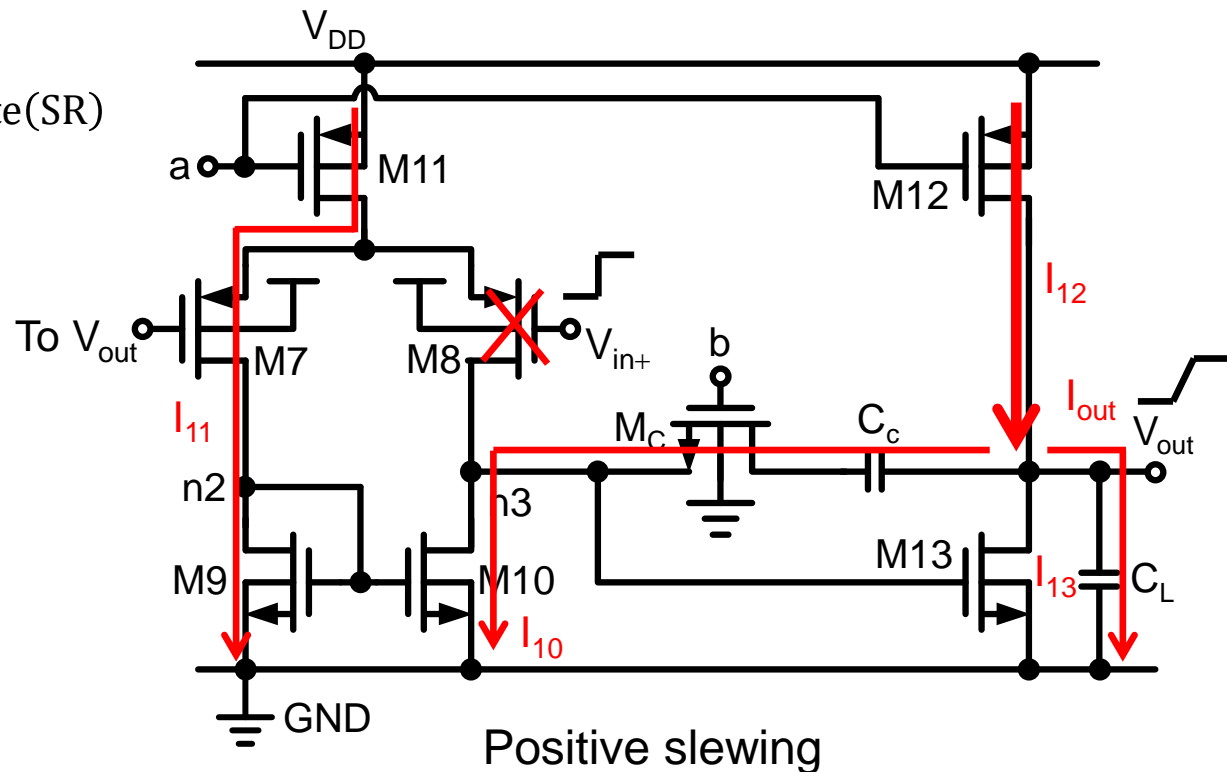
- 講義6-29, 6-30所推得結果:  $\text{Slew rate}(\text{SR}) = \frac{I_{11}}{C_C} \rightarrow$  不完全適用於這次作業

- ◆ 因為講義上之範例，第二級為ideal OP且無 $C_L$
- ◆ 當 $I_{12}$ 足夠大  $\rightarrow \text{Slew rate}(\text{SR}) = \frac{I_{11}}{C_C}$
- ◆ 當 $I_{12}$ 不夠大  $\rightarrow \text{Slew rate}(\text{SR}) < \frac{I_{11}}{C_C} \ \& \ \frac{I_{12}}{C_C + C_L}$



- Rising & Falling 之 Slew rate(SR)

- ◆ 都必須測試且附上波形





# Appendix 4: 電腦教室C18帳號申請 & 使用說明

- 1. 有需要申請電腦教室帳號的同學，請至moodle申請。
  - ◆ 請同學第一次登入時，以passwd指令修改密碼，以免被他人盜用。
- 2. 使用CIC 0.18 $\mu$ m 1.8V SPICE Model (cic018.l)
- 3. 請在testbench中輸入以下指令以取得製程權限。

```
.protect  
.lib '/home/ncku_class/AIC_class_2025/analog2300/cic018.l' tt  
unprotect
```
- 4. 使用hspice以及spice explorer前
  - ◆ 請於自己的資料夾開啟terminal
  - ◆ 輸入: source /home/ncku\_class/AIC\_class\_2025/analog2300/setup.cshrc
  - ◆ 直到出現成功訊息: set hspice version ....
- 5. 執行hspice之指令：hspice -i test.sp -o test.lis
- 6. 執行virtuoso之指令：virtuoso
- 7. 執行waveview之指令：wv

# Appendix 4: 電腦教室ADFP帳號申請 & 使用說明

- 1. 有需要申請電腦教室帳號的同學，請至moodle申請。
  - ◆ 請同學第一次登入時，以passwd指令修改密碼，以免被他人盜用。

- 2. 使用ADFP 16nm 1.0V SPICE Model (cic018.l)
- 3. 請在testbench中輸入以下指令以取得製程權限。

```
.protect
```

```
.lib '/usr/cad/CBDK/Executable_Package/Collaterals/Tech/SPICE/N16ADFP_SPICE_MODEL/n16adfp_spice_model_v1d0_usage.l' TTMacro_MOS_MOSCAP
```

```
.unprotect
```

- 4. 使用hspice以及spice explorer前
  - ◆ 請於自己的資料夾開啟terminal
  - ◆ 輸入: source /home/user1/analog25/analog2501/setup.cshrc
  - ◆ 直到出現成功訊息: set hspice version ....

- 5. 執行hspice之指令：hspice -i test.sp -o test.lis

- 6. 執行virtuoso之指令：virtuoso

- 7. 執行waveview之指令：wv

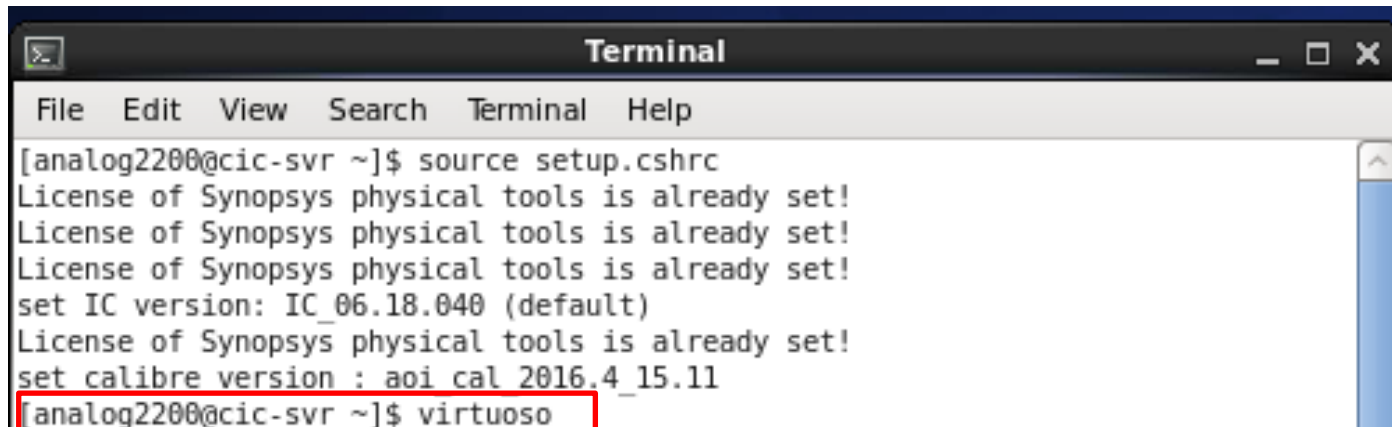
# Cadence Virtuoso Schematic Guide

# Outline

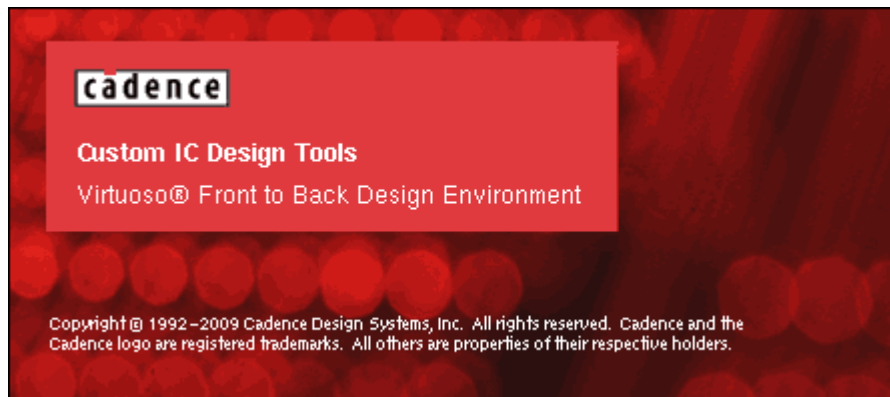
- Launch Cadence Virtuoso
- Create a new library
- Create a new cell
- Construction of circuit
  - ◆ Instances
  - ◆ Wires and pins
  - ◆ Voltage sources
  - ◆ Example
- Export circuits
- HSPICE verification

# Launch Cadence Virtuoso

- Step 1: Launch terminal
- Step 2: Command “virtuoso”

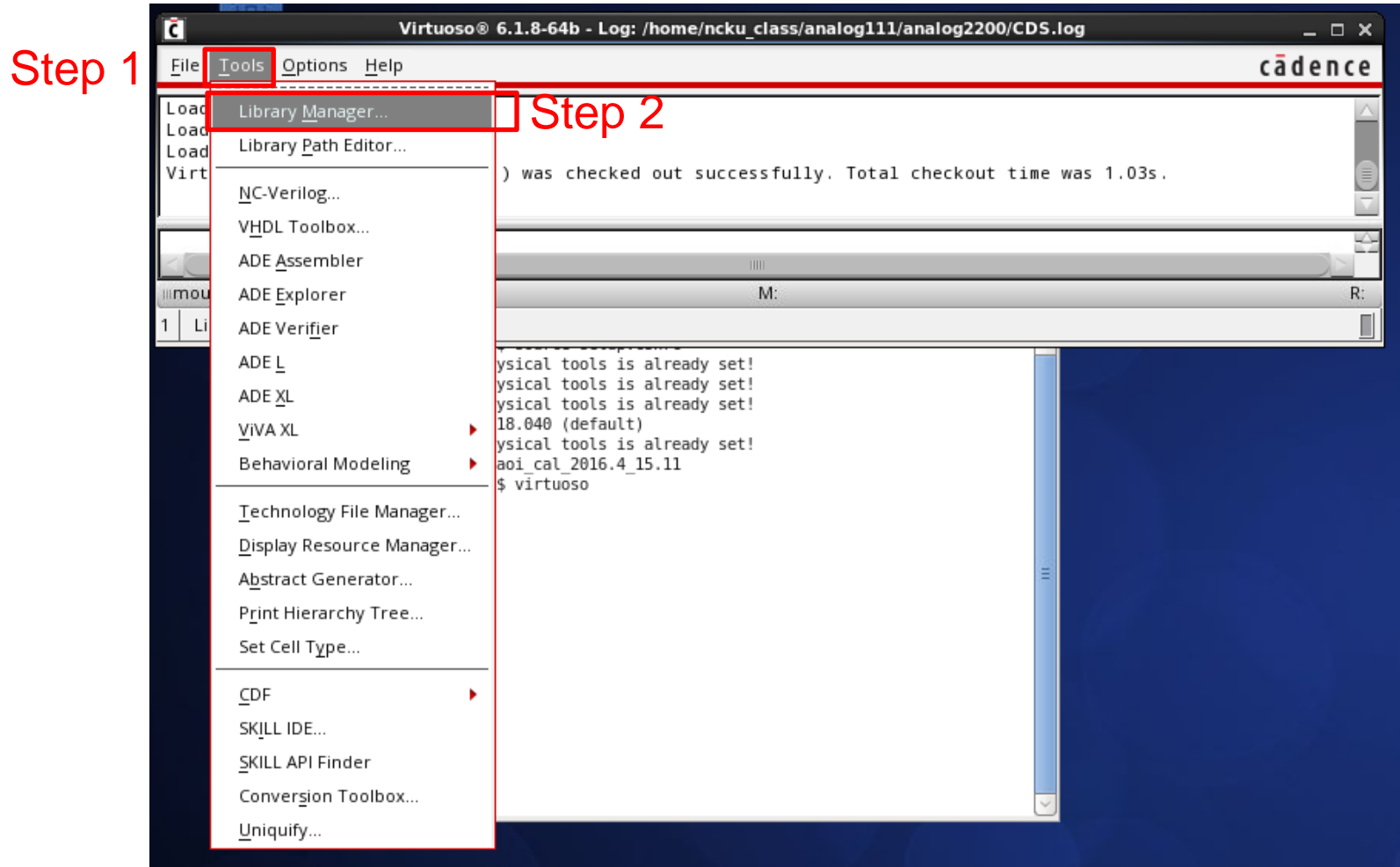


```
Terminal
File Edit View Search Terminal Help
[analog2200@cic-svr ~]$ source setup.cshrc
License of Synopsys physical tools is already set!
License of Synopsys physical tools is already set!
License of Synopsys physical tools is already set!
set IC version: IC_06.18.040 (default)
License of Synopsys physical tools is already set!
set calibre version : aoi cal 2016.4_15.11
[analog2200@cic-svr ~]$ virtuoso
```



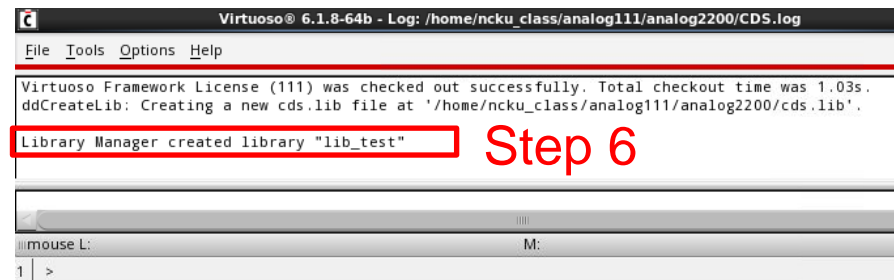
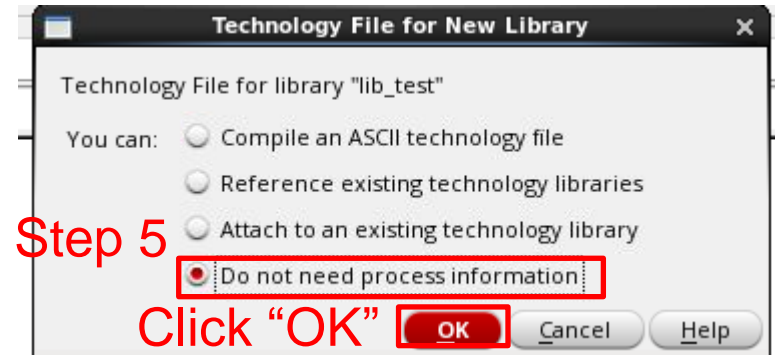
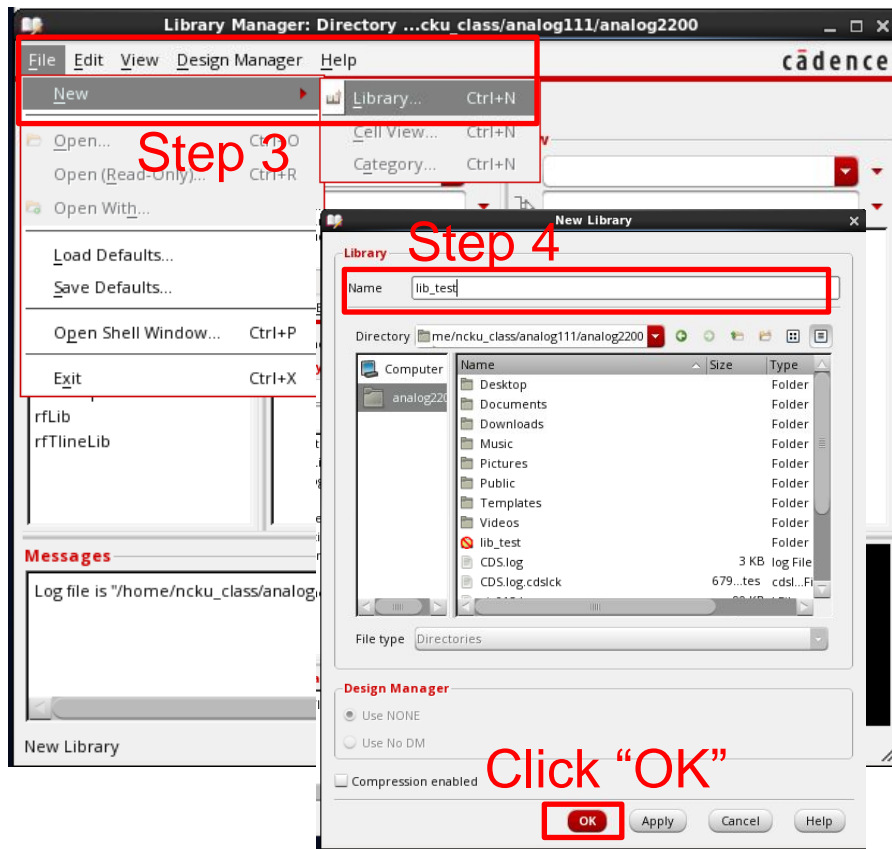
# Create a New Library (1/2)

- Step 1: Select “Tools”
- Step 2: Select “Library Manager”



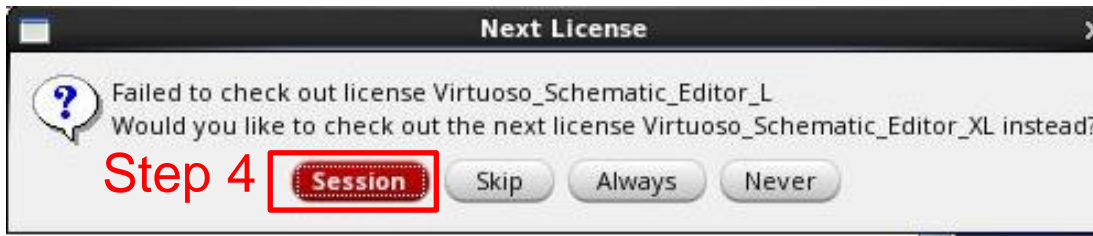
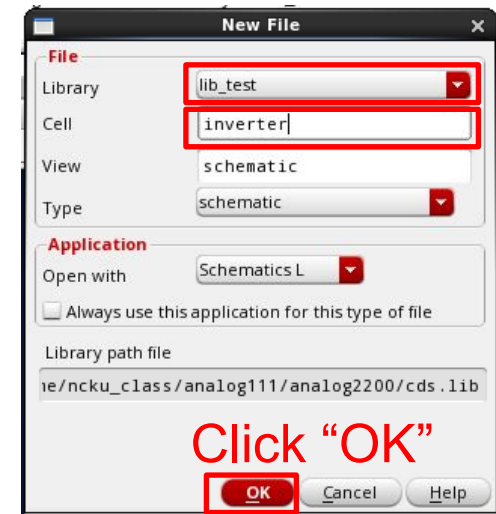
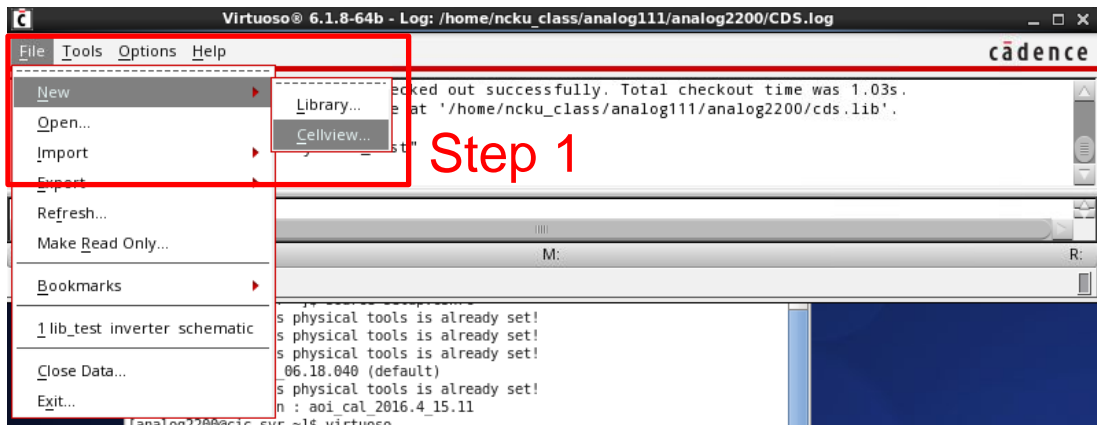
# Create a New Library (2/2)

- Under Library Manager
  - ◆ Step 3: Select “File>New>Library”
  - ◆ Step 4: Name your new library
  - ◆ Step 5: Choose “Don’t need a techfile”
  - ◆ Step 6: Check new library is actually created



# Create a New Cell

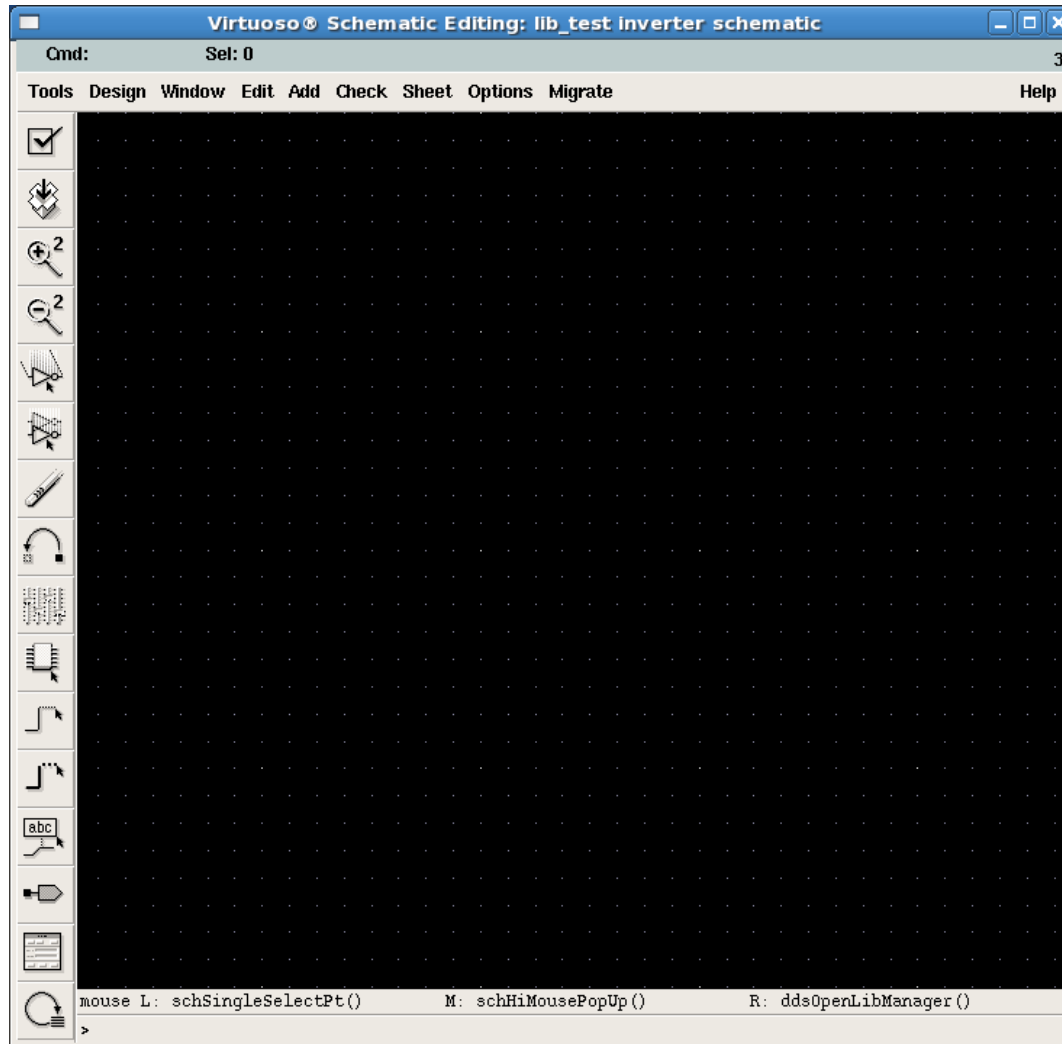
- Under Library Manager
  - ◆ Step 1: Select “File>New>Cell View”
  - ◆ Step 2: Select your library
  - ◆ Step 3: Name your new cell
  - ◆ Step 4: Click “Session”





## Construction of Circuit

- After creating a new cell, the schematic will automatically pump up.



## Construction of Circuit: Instances (1/2)

- Step 1: Select “Create>Instance” (Hotkey:”i”)
- Step 2: Click “Browse”
- Step 3: Choose “analogLib” library
- Step 4: Select required cells
- Step 5: Choose “symbol” in view

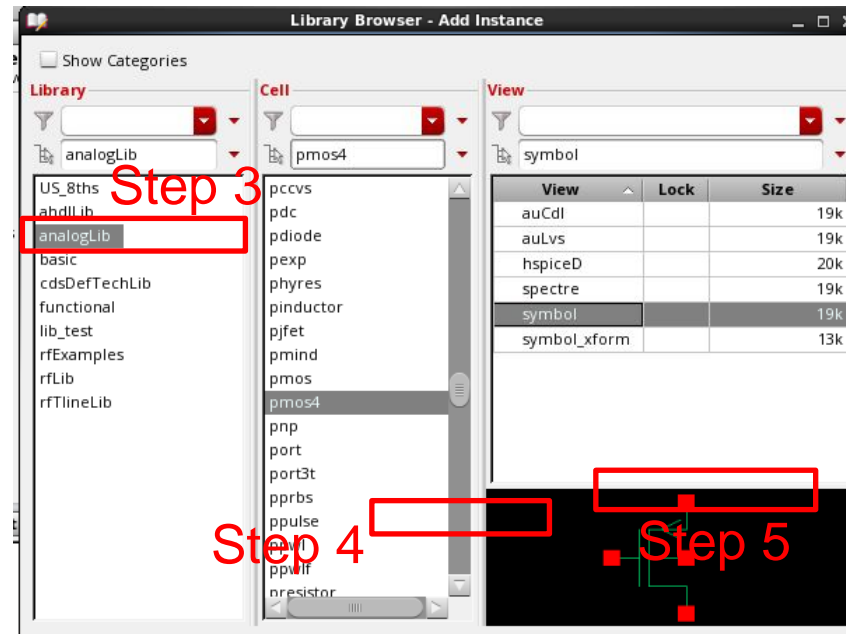
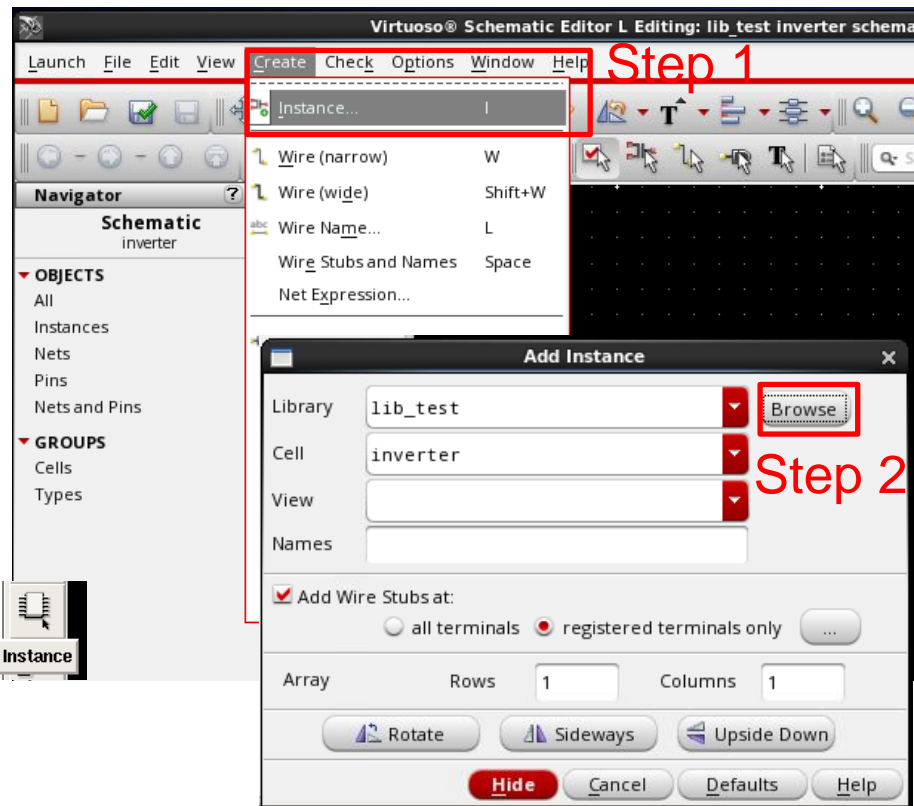
## Popular cells:

Capacitor: “cap”

## Resistor: “res”

NMOS: “nmos4”

PMOS: “pmos4”



# Construction of Circuit: Instances (2/2)

- Step 6: Edit instance property (Example: pmos4)

**Name**

**Device definition in 180nm (16nm)**

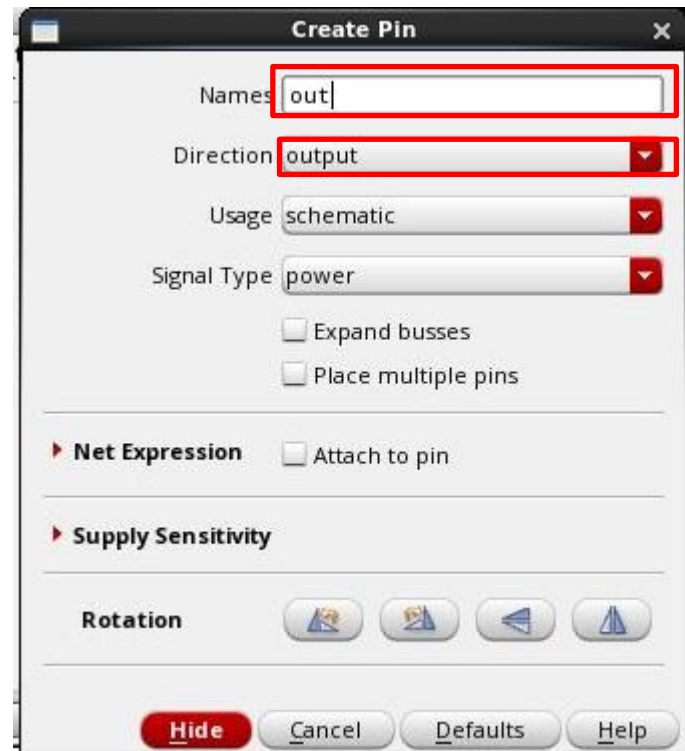
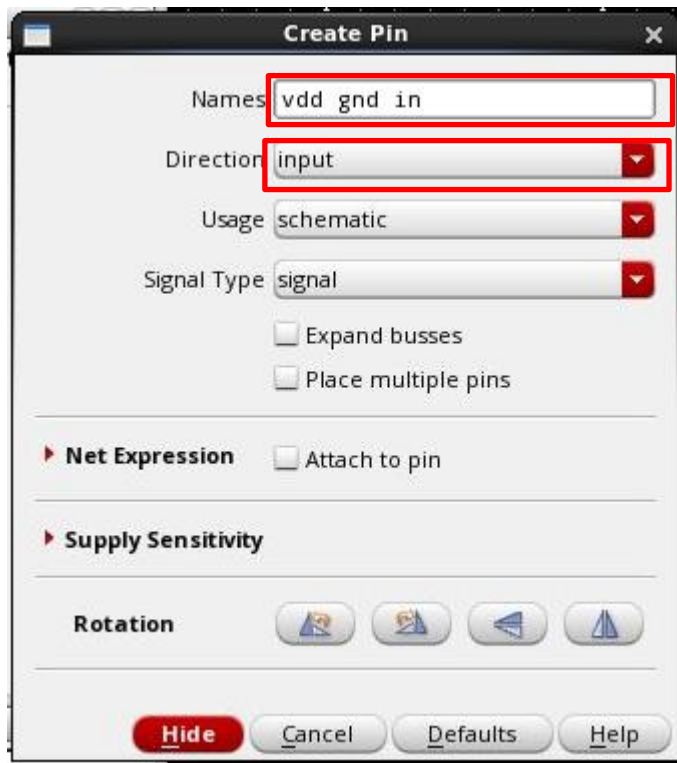
**Symbol**

Property	Value	Display
Library Name	analogLib	off
Cell Name	pmos4	off
View Name	symbol	off
Instance Name	mp1	off

Model name	Value	Display
Model name	p_18 (pch_svt_mac)	off
Width	250n M (Number of fin, e.g. 2)	off
Length	180n M	off

# Construction of Circuit: Wires and Pins

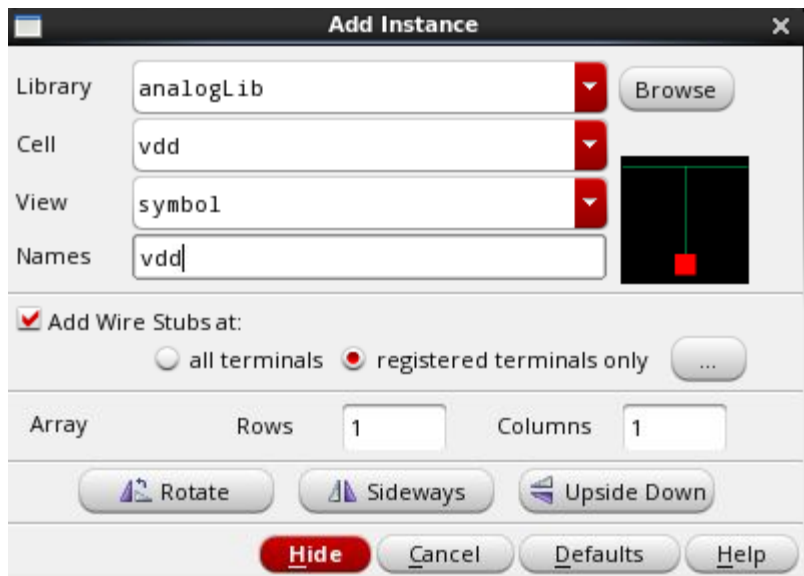
- Add wire: “w” (Hotkey)
  - ◆ Select two nodes to wire each other
- Add pin: “p” (Hotkey)
  - ◆ Name: Defined by designer
  - ◆ Direction: input/output



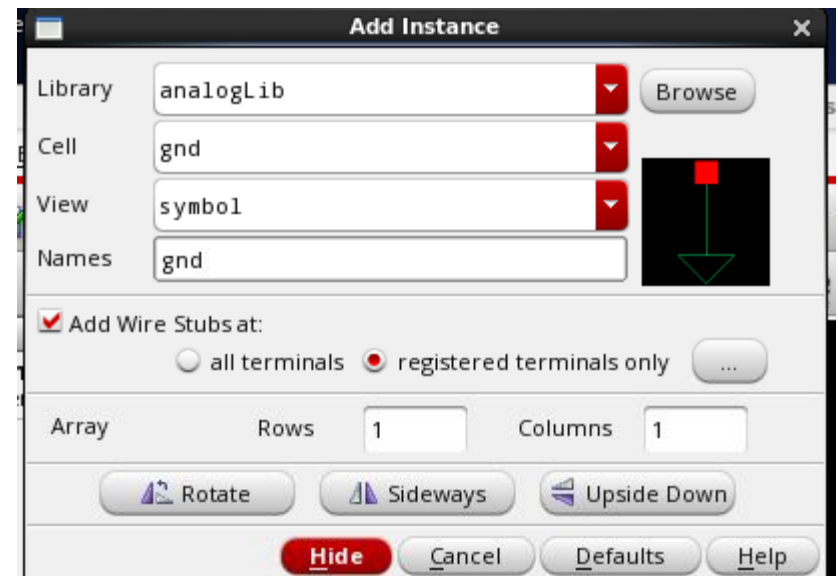
# Construction of Circuit: Voltage Sources

- Step 1: Choose “analogLib” library
- Step 2: Select required voltage sources
- Step 3: Choose “symbol” in view

vdd



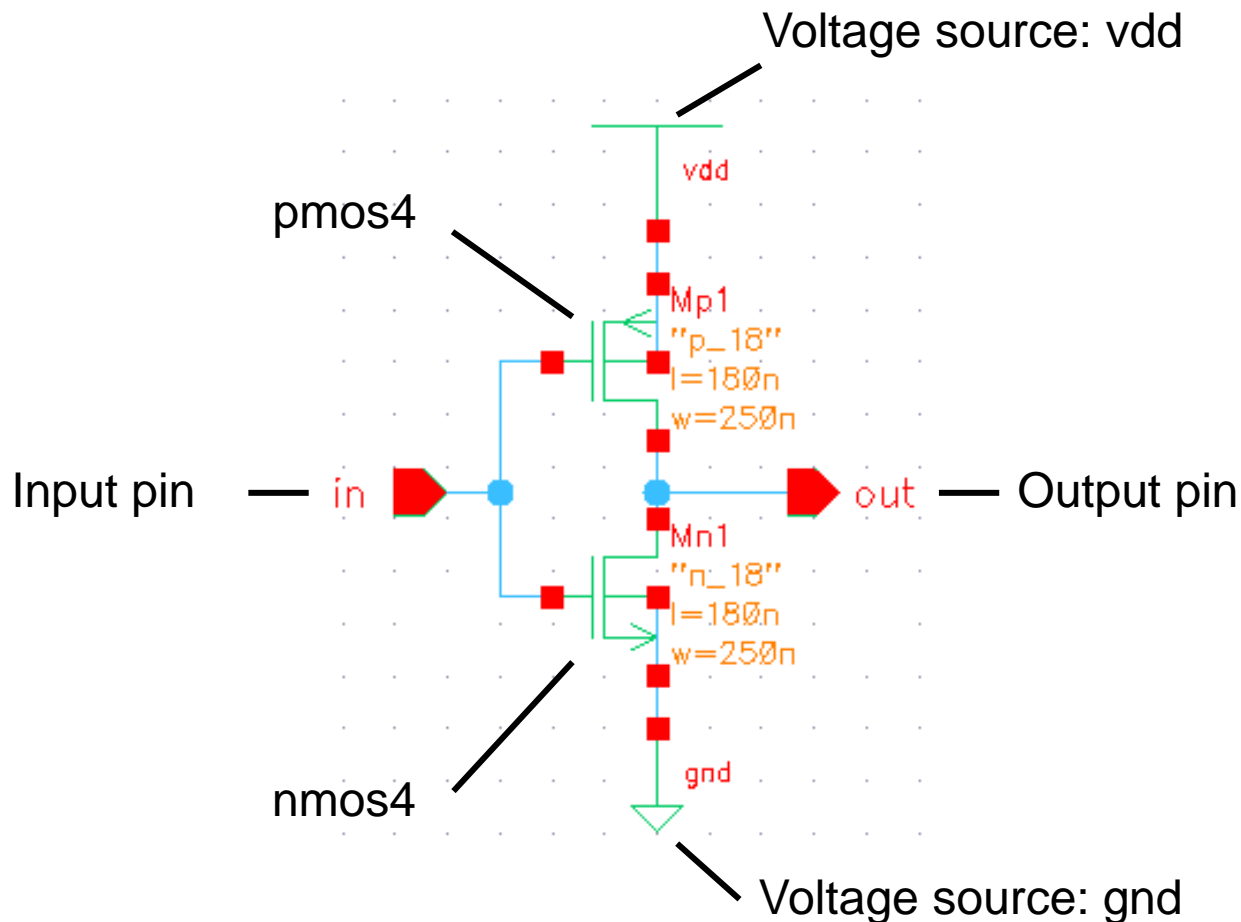
gnd



# Construction of Circuit: Example

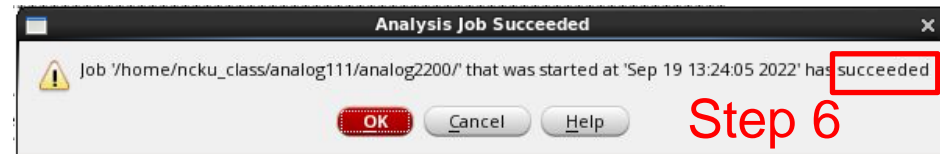
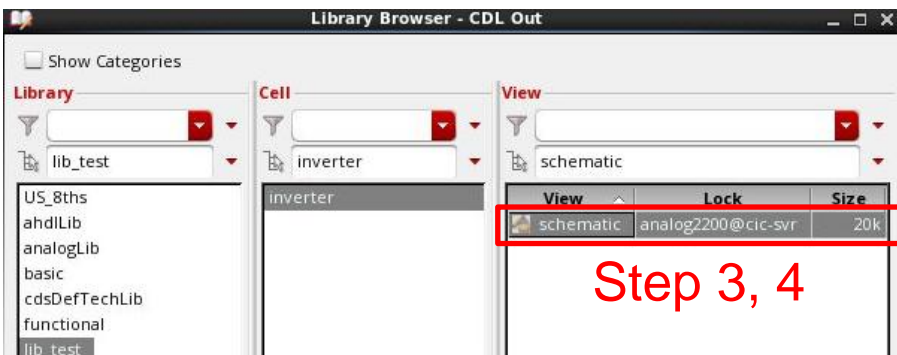
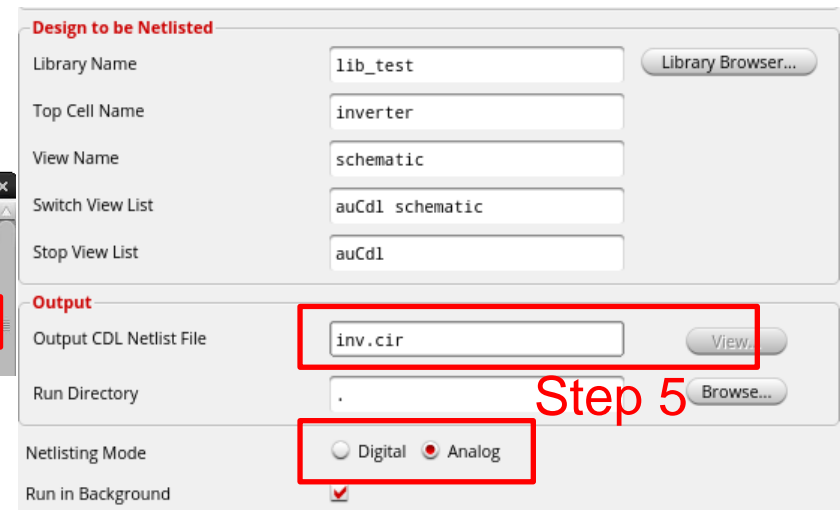
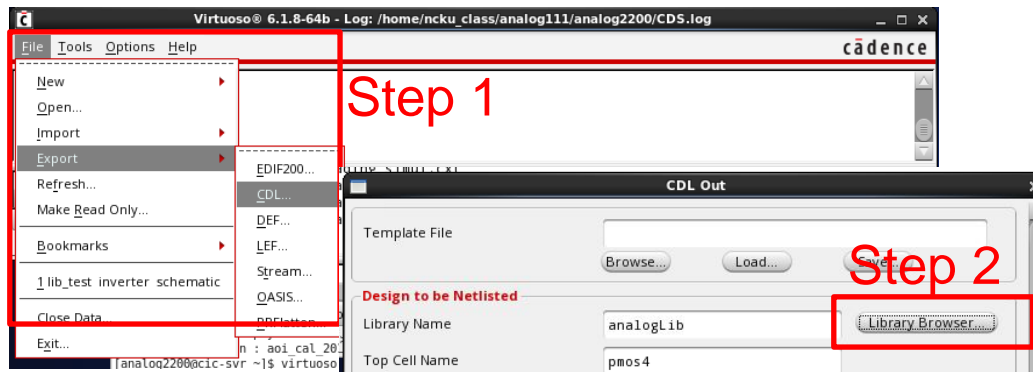
- Circuit example: Inverter

Save your circuit: "Shift+x" (Hotkey)



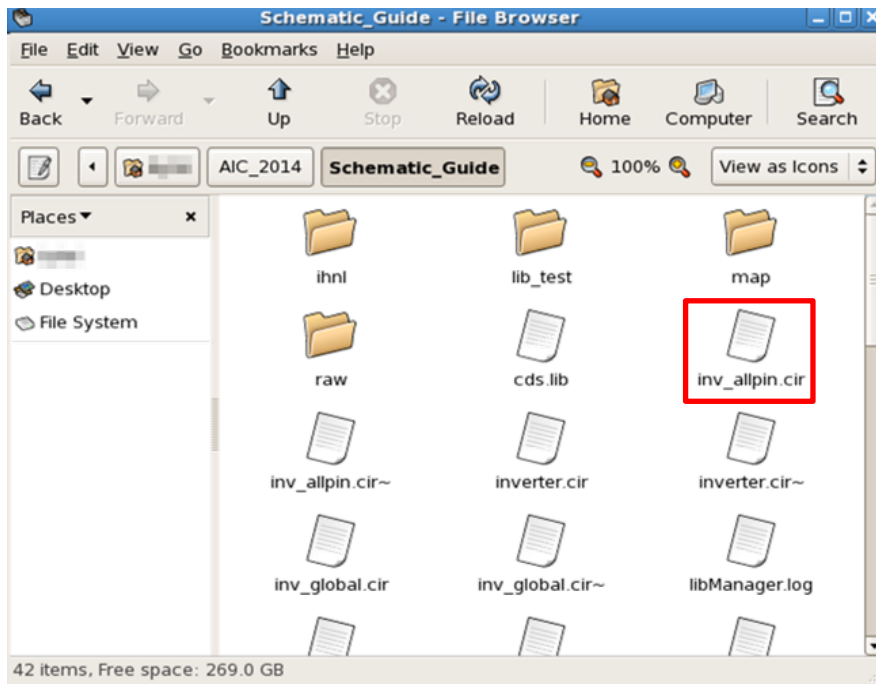
# Export Circuits

- Step 1: Select “File>Export>CDL”
- Step 2: Click “Library Browser”
- Step 3: Select required cell
- Step 4: Select “schematic” in view
- Step 5: Name your output file (Filename extension: .cir) and select “Analog”
- Step 6: Check the exportation is successful



# HSPICE Verification for 180nm (1/2)

- Step 1: Find the exported file (.cir file)
- Step 2: Re-define voltage sources
  - ◆ If you define vdd and gnd as **pins**: Jump to next page to continue
  - ◆ If you define vdd and gnd as **voltage sources**
    - Step 2-1: Delete definition of voltage sources
    - Step 2-2: Replace “vdd!(gnd!)” to “vdd(gnd)”
    - Step 2-3: Add “vdd” and “gnd” as pins



.GLOBAL gnd!  
+ vdd!

**Step 2-1**

```
*****
* Library Name: lib_test
* Cell Name: inverter
* View Name: schematic
*****

.SUBCKT inverter in out
*.PININFO in:I out:O
MMp1 out in vdd! vdd! PM W=250n L=180n
MMn1 out in gnd! gnd! NM W=250n L=180n
.ENDS
```

**Step 2-2**

```
.SUBCKT inverter in out vdd gnd
*.PININFO in:I out:O
MMp1 out in vdd vdd PM W=250n L=180n
MMn1 out in gnd gnd NM W=250n L=180n
.ENDS
```

**Step 2-3**



# HSPICE Verification for 180nm (2/2)

- Step 3: Replace devices name ( PM → P\_18 ; NM → N\_18 )

```
*****
* Library Name: lib_test
* Cell Name: inverter
* View Name: schematic
*****
.SUBCKT inverter in out vdd gnd
*.PININFO gnd:I in:I vdd:I out:O
MMp1 out in vdd vdd PM W=250n L=180n
MMn1 out in gnd gnd NM W=250n L=180n
.ENDS
```

```
.SUBCKT inverter in out vdd gnd
*.PININFO gnd:I in:I vdd:I out:O
MMp1 out in vdd vdd P_18 W=250n L=180n
MMn1 out in gnd gnd N_18 W=250n L=180n
.ENDS
```

Step 3

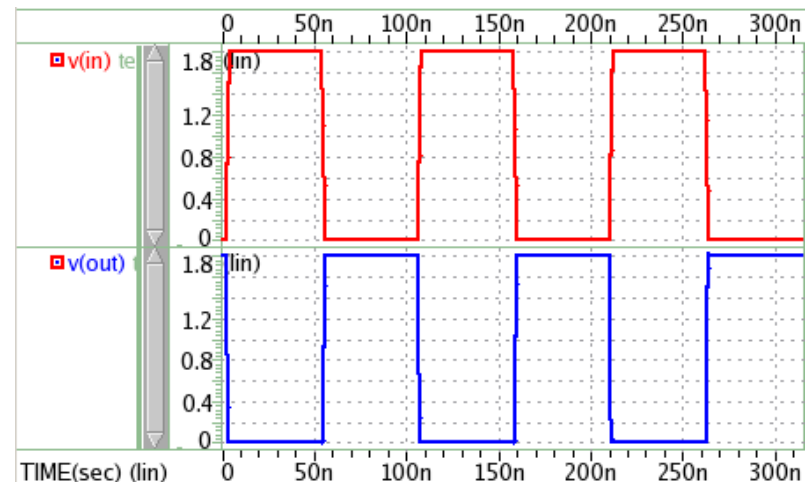
P.S. The **pin order** of the SUBCKT should be checked which must be the same as the one in testbench!

- Step 4: Include your circuit in HSPICE testbench
- Step 5: Run simulation and verification

```
.protect
.lib '/home/ncku_class/AIC_class_2025/analog2300/cic018.l' tt
.unprotect

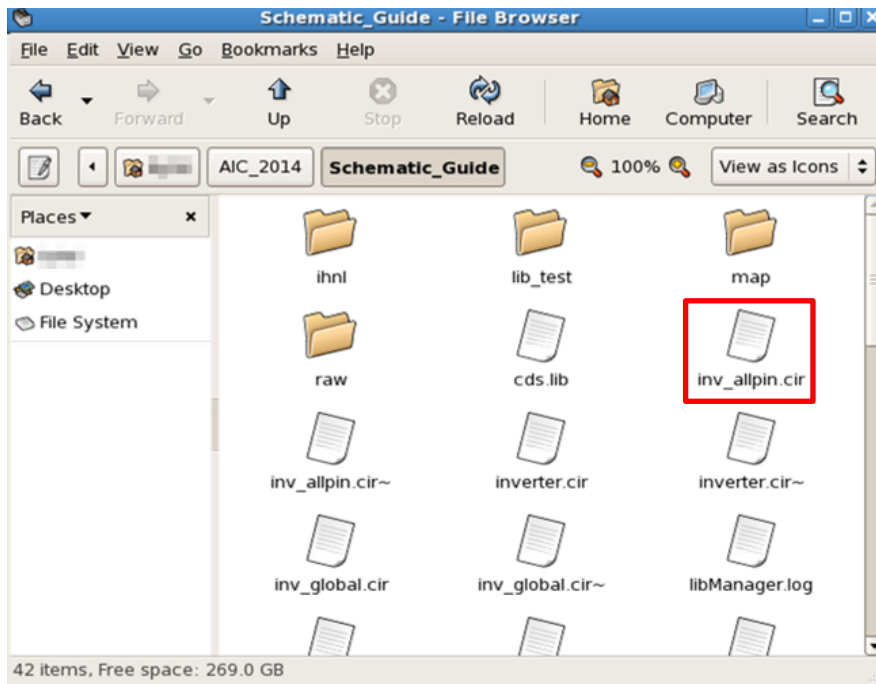
.include 'inv_allpin.cir'
Vvdd vdd 0 1.8
Vin in 0 pulse(0 1.8 2n 2n 2n 50n 104n)
Xinv in out vdd gnd inverter
.tran 1p 314n
.option post
.end
```

Step 4



# HSPICE Verification for 16nm (1/2)

- Step 1: Find the exported file (.cir file)
- Step 2: Re-define voltage sources
  - ◆ If you define vdd and gnd as **pins**: Jump to next page to continue
  - ◆ If you define vdd and gnd as **voltage sources**
    - Step 2-1: Delete definition of voltage sources
    - Step 2-2: Replace “vdd!(gnd!)” to “vdd(gnd)”
    - Step 2-3: Add “vdd” and “gnd” as pins



.GLOBAL gnd!  
+ vdd! Step 2-1

```
*****
* Library Name: lib_test
* Cell Name: inverter
* View Name: schematic
*****

.SUBCKT inverter in out
*.PININFO in:I out:O
MMp1 out in vdd! vdd! PM nfin=1 L=16n
MMn1 out in gnd! gnd! NM nfin=1 L=16n
.ENDS
```

Step 2-2

```
.SUBCKT inverter in out vdd gnd
*.PININFO in:I out:O
MMp1 out in vdd vdd PM nfin=1 L=16n
MMn1 out in gnd gnd NM nfin=1 L=16n
.ENDS
```

Step 2-3

# HSPICE Verification for 16nm (2/2)

- Step 3: Replace devices name ( PM → pch\_svt\_mac ; NM → nch\_svt\_mac ; W→nfin)

*\*This is an example, you can decide which model to use*

```
*****
* Library Name: lib_test
* Cell Name: inverter
* View Name: schematic
*****
.SUBCKT inverter in out vdd gnd
*.PININFO gnd:I in:I vdd:I out:O
MMp1 out in vdd vdd PM W=2 L=16n
MMn1 out in gnd gnd NM W=2 L=16n
.ENDS
```

```
.SUBCKT inverter in out vdd gnd
*.PININFO gnd:I in:I vdd:I out:O
MMp1 out in vdd vdd pch_svt_mac nfin=2 L=16n
MMn1 out in gnd gnd nch_svt_mac nfin=2 L=16n
.ENDS
```

Step 3

P.S. The **pin order** of the SUBCKT should be checked which must be the same as the one in testbench!

- Step 4: Include your circuit in HSPICE testbench
- Step 5: Run simulation and verification

```
.protect
.lib
'/usr/cad/CBDK/Executable_Package/Collaterals/Tech/SPICE/N
16ADFP_SPICE_MODEL/n16adfp_spice_model_v1d0_usage.l'
TTMacro_MOS_MOSCAP
.unprotect
.include 'inv_allpin.cir'
Vvdd vdd 0 1
Vin in 0 pulse(0 1 2n 2n 2n 50n 104n)
Xinv in out vdd gnd inverter
.tran 1p 314n
.option post
.end
```

Step 4

\*Power Source\*  
 \*Input Signal\*  
 \*Call Subckt\*  
 \*Transient Analysis\*

